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Washington, D.C. 20231

Re: Inventor(s): FREDERIC GAILLARD; LI-QUAN XIA; ELLIE YIEH; PAUL FISHER and MARGARET GOTUACO
Title: NOVEL INTEGRATION SCHEME FOR DUAL DAMASCENE STRUCTURE

Transmitted herewith is the patent application identified above, including:

X Specification, claims and abstract, totaling 28 pages.

X Drawings totaling 5 pages, X Formal ___ Informal.

X Executed Declaration and Power of Attorney.

_ Information Disclosure Statement w/ Form 1449 and References.

X Assignment of the invention to **Applied Materials, Inc.**

X Assignment Recordation Cover Sheet

FEE CALCULATION

Fee Items	Claims Filed	Included With Basic Fee	Extra Claims	Fee Rate	Total
Total Claims	60	-20=	40	x $18.00	$ 720.00
Independent Claims	3	-3=	0	x $80.00	$ 0.00
Basic Filing Fee				$710.00	$ 710.00
TOTAL FEES					$1430.00

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UNITED STATES PATENT APPLICATION FOR:

NOVEL INTEGRATION SCHEME FOR DUAL DAMASCENE STRUCTURE

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Certification Under 37 CFR 1.10

I hereby certify that this New Application and the documents referred to as enclosed therein are being deposited with the United States Postal Service on 11-03-2000, in an envelope marked as "Express Mail United States Postal Service", Mailing Label No. EL684620563, addressed to: Assistant Commissioner for Patents, Box PATENT APPLICATION, Washington, D.C. 20231.

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NOVEL INTEGRATION SCHEME FOR DUAL DAMASCENE STRUCTURE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to the fabrication of integrated circuits and to a process and apparatus for forming semiconductor devices on a substrate.

Background of the Related Art

Consistent and fairly predictable improvement in integrated circuit (IC) design and fabrication has been observed in the last decade. One key to successful improvements in IC design and fabrication is the multilevel interconnect technology which provides the conductive paths in an IC device. The shrinking dimensions of conductive or semiconductive substrate features such as horizontal lines and vertical contacts, vias, or interconnects, in very large scale integration (VLSI) and ultra large scale integration (ULSI) technology, has increased the importance of improving the current density of semiconductor devices.

In order to further improve the current density of semiconductor devices on integrated circuits, it has become necessary to use conductive materials having low resistivity and low dielectric constant (low k) materials (defined herein as having dielectric constants, k, less than about 4.0) as insulating layers to reduce the capacitive coupling between adjacent interconnects. Increased capacitative coupling between layers can detrimentally affect the functioning of semiconductor devices.

However, typical low k dielectric materials are generally porous and generally require a barrier layer to prevent interlayer diffusion of materials into the low k dielectric materials. The barrier layer comprises conventional barrier materials, such as silicon oxide and silicon nitride, that have dielectric constants greater than 4.0 and often greater than 7.0. The resulting insulator stack of low k dielectric materials and conventional barrier materials may have a dielectric constant that is not much below 6.0 which minimizes the use of low k dielectric materials as intermetal dielectric layers.

Copper is also being used to improve the current density of semiconductor devices. Copper (Cu) is becoming the interconnect material of choice because of copper's low

resistivity (1.7 μΩ-cm) and high current carrying capacity. However, copper diffuses more readily into surrounding materials and can alter the electronic device characteristics of the adjacent layers and, for example, form a conductive path between layers, thereby reducing the reliability of the overall circuit and may even result in device failure.

One additional difficulty in using copper in semiconductor devices is that copper is difficult to etch and achieving precise pattern etching with copper using traditional deposition/etch processes for forming interconnects has been less than satisfactory. Further, the etch processes of low k materials, such as silicon carbide (SiC) and carbon doped silicon oxides, have not been well quantified and qualified in the art. Thus, the combination of low k materials and copper has led to new deposition methods for preparing semiconductor features, such as vertical and horizontal interconnects, since copper is not easily etched to form metal lines. One method is the damascene or dual damascene methods depositing vertical and horizontal interconnects, wherein one or more dielectric materials are deposited and pattern etched to form the vertical and horizontal interconnects. Conductive materials, such as copper and other metals, are then inlaid into the etched pattern and any excess metal is removed from the top of the structure in a planarization process, such as chemical mechanical polishing (CMP).

However, low k dielectric materials often have a less than desirable hardness. Hardness is defined herein as a stability of a material during processing for retention of its shape or form. If low k dielectric materials disposed adjacent the dual damascene structure lacks sufficient hardness, the dual damascene structures may be imprecisely formed and can deform during latter processing of the substrate. For example, CMP can exert force against the dielectric material disposed on the substrate surface, which can distort the dielectric material, and in some cases result in delamination of the dielectric material from the substrate. Also, the low k dielectric materials are porous and processing, such as chemical mechanical polishing, can compress the porous dielectric material and increase the k value.

Additionally, it has been observed that dual damascene structures formed in low k materials have greater mechanical stresses than structures formed in traditional dielectric materials. Greater mechanical stresses can lead to imprecise formation of the dual damascene structure and increased deformation of the dual damascene structure during processing. Deformation or malformation of the dual damascene structures can detrimentally affect the performance of semiconductor devices.

Therefore, there is a need for an improved process for forming dual damascene structures with low k dielectric material. Ideally the low k dual damascene structure has good hardness and can be formed without the presence of barrier layers or etch-stops.

SUMMARY OF THE INVENTION

The invention generally relates to a method and apparatus for processing a substrate to form a feature in low k dielectric materials. One aspect of the invention provides a method for forming a feature in a low k dielectric material including forming a feature definition in a dielectric material deposited on a surface of a substrate, depositing one or more conductive materials to fill at least a portion of the feature definition, planarizing the substrate surface to expose the dielectric material, removing at least a portion of the dielectric material, and depositing a low k dielectric material.

Another aspect of the invention provides a method for forming a dual damascene interconnect comprising depositing one or more dielectric layers on a substrate, etching the one or more dielectric layers to form the dual damascene definition, the dual damascene definition having a vertical and a horizontal interconnect, depositing a conductive barrier layer over the exposed services of a dual damascene definition, depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition, planarizing the filled dual damascene definition to expose the one or more dielectric layers, removing at least a portion of the one or more dielectric layers, depositing a low k dielectric material, and depositing a self-planarizing dielectric material on the low k dielectric layer.

Another aspect of the invention provides a method for forming a dual damascene interconnect, comprising depositing a first dielectric material, depositing a second dielectric material on the first dielectric material, etching the second dielectric layer to exposed a portion of the first dielectric layer, depositing a third dielectric layer on the second dielectric material and exposed portion of the first dielectric layer, etching the first and third dielectric layers to form a vertical interconnect and a horizontal interconnect of a dual damascene definition, depositing a conductive barrier layer over exposed surfaces of the dual damascene definition, depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition, planarizing the filled dual damascene definition to expose the one or more dielectric layers, removing the one or more dielectric

layers, depositing a low k dielectric material on the substrate, and depositing a self-planarizing dielectric layer on the low k dielectric material.

BRIEF DESCRIPTION OF THE DRAWINGS

So that the manner in which the above recited features, advantages and objects of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

Figure 1 is a cross sectional diagram of one embodiment of an exemplary chemical vapor deposition (CVD) chamber for performing one or more processing steps described herein;

Figure 2 is a flow chart illustrating steps is a flow chart illustrating steps of one embodiment in forming a dual damascene structure; and

Figures 3A to 3H are schematic diagrams of one embodiment of a process for fabricating a dual damascene structure.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The invention will be described below in reference to forming a feature in low k dielectric material. Generally, the method includes forming a feature in a dielectric material deposited on a surface of a substrate, removing at least a portion of the deposited dielectric material, and depositing a low k dielectric material, preferably as a gap fill, on the substrate surface.

The dielectric material and low dielectric material are preferably deposited by chemical vapor deposition. A suitable chemical vapor deposition plasma chamber for depositing dielectric materials is a DxZ ™ CVD chamber commercially available for Applied Material, Inc., located in Santa Clara, California. The DxZ™ CVD chamber can be included on integrated platform such as the Endura ™ platform available from Applied Materials, Inc. located in Santa Clara, California. The deposition of dielectric materials may occur in a variety of chambers and the DxZ™ chamber described herein is provided for

illustrative purposes, and should not be so construed or interpreted as to limit the scope of the invention.

Figure 1 shows a vertical, cross-section view of a parallel plate chemical vapor deposition reactor 110 having a high vacuum region 115. The reactor 110 contains a gas distribution manifold 111 for dispersing process gases through perforated holes in the manifold to a substrate or substrate (not shown) that rests on a substrate support plate or susceptor 112 which is raised or lowered by a lift motor 114. A liquid injection system (not shown), such as typically used for liquid injection of TEOS, may also be provided for injecting a liquid organosilicon compound.

The reactor 110 includes heating of the process gases and substrate, such as by resistive heating coils (not shown) or external lamps (not shown). Referring to Fig. 1, susceptor 112 is mounted on a support stem 113 so that susceptor 112 (and the substrate supported on the upper surface of susceptor 112) can be controllably moved between a lower loading/off-loading position and an upper processing position which is closely adjacent to manifold 111.

When susceptor 112 and the substrate are in processing position 114, they are surrounded by a an insulator 117 and process gases exhaust into a manifold 124. During processing, gases inlet to manifold 111 are uniformly distributed radically across the surface of the substrate. A vacuum pump 132 having a throttle valve controls the exhaust rate of gases from the chamber.

Before reaching manifold 111, deposition and carrier gases are input through gas lines 118 into a mixing system 119 where they are combined and then sent to manifold 111. Generally, the process gases supply line 118 for each of the process gases also includes (i) safety shut-off valves (not shown) that can be used to automatically or manually shut off the flow of process gas into the chamber, and (ii) mass flow controllers (also not shown) that measure the flow of gas through the gas supply lines. When toxic gases are used in the process, several safety shut-off valves are positioned on each gas supply line in conventional configurations.

The deposition process performed in reactor 110 can be either a thermal process or a plasma enhanced process. In a plasma process, a controlled plasma is typically formed adjacent to the substrate by RF energy applied to distribution manifold 111 from RF power supply 125 (with susceptor 112 grounded). Alternatively, RF power can be provided to the

susceptor 112 or RF power can be provided to different components at different frequencies. RF power supply 125 can supply either single or mixed frequency RF power to enhance the decomposition of reactive species introduced into the high vacuum region 115. A mixed frequency RF power supply typically supplies power at a high RF frequency (RF1) of 13.56 MHz to the distribution manifold 111 and at a low RF frequency (RF2) of 360 KHz to the susceptor 112. The silicon oxide layers of the present invention are most preferably produced using low levels of constant high frequency RF power or pulsed levels of high frequency RF power.

When additional dissociation of the oxidizing gas is desired, an optional microwave chamber 128 can be used to input from between about 0 Watts and about 6000 Watts of microwave power to the oxidizing gas prior to entering the deposition chamber. Separate addition of microwave power would avoid excessive dissociation of the organosilicon compounds prior to reaction with the oxidizing gas. A gas distribution plate having separate passages for the organosilicon compound and the oxidizing gas is preferred when microwave power is added to the oxidizing gas.

Typically, any or all of the chamber lining, distribution manifold 111, susceptor 112, and various other reactor hardware is made out of material such as aluminum or anodized aluminum. An example of such a CVD reactor is described in U.S. Patent 5,000,113, entitled "A Thermal CVD/PECVD Reactor and Use for Thermal Chemical Vapor Deposition of Silicon Dioxide and *In-situ* Multi-step Planarized Process," issued to *Wang et al.* and assigned to Applied Materials, Inc., the assignee of the present invention.

The lift motor 114 raises and lowers susceptor 112 between a processing position and a lower, substrate-loading position. The motor, the gas mixing system 119, and the RF power supply 125 are controlled by a system controller 134 over control lines 136. The reactor includes analog assemblies, such as mass flow controllers (MFCs) and standard or pulsed RF generators, that are controlled by the system controller 134 which executes system control software stored in a memory 138, which in the preferred embodiment is a hard disk drive. Motors and optical sensors are used to move and determine the position of movable mechanical assemblies such as the throttle valve of the vacuum pump 132 and motor for positioning the susceptor 112.

The system controller 134 controls all of the activities of the CVD reactor and a preferred embodiment of the controller 134 includes a hard disk drive, a floppy disk drive,

and a card rack. The card rack contains a single board computer (SBC), analog and digital input/output boards, interface boards and stepper motor controller boards. The system controller conforms to the Versa Modular Europeans (VME) standard which defines board, card cage, and connector dimensions and types. The VME standard also defines the bus structure having a 16-bit data but and 24-bit address bus.

The system controller 134 operates under the control of a computer program stored on the hard disk drive 138. The computer program dictates the timing, mixture of gases, RF power levels, susceptor position, and other parameters of a particular process. The above CVD system description is mainly for illustrative purposes, and other plasma CVD equipment such as electrode cyclotron resonance (ECR) plasma CVD devices, induction-coupled RF high density plasma CVD devices, or the like may be employed. Additionally, variations of the above described system such as variations in susceptor design, heater design, location of RF power connections and others are possible. For example, the substrate could be supported and heated by a resistively heated susceptor. The pretreatment and method for forming a pretreated layer of the present invention is not limited to any specific apparatus or to any specific plasma excitation method.

Feature Formation

Generally, a feature, such as a dual damascene structure, is formed by depositing dielectric material on the surface of a substrate, etching the dielectric material to form a feature definition, filling at least a portion of the feature definition with conductive material to form the feature, planarizing the feature, removing at least a portion of the dielectric material in which the feature is formed, and then depositing a low k dielectric material on the substrate surface. The dielectric material may comprise one or more dielectric layers. The feature formed is preferably a dual damascene structure. The low k dielectric layer is preferably deposited to cover the dual damascene structure and to fill in gaps and voids formed during the dielectric material removal process, such as by a gap fill process.

While the following description detailed herein is directed to the formation of dual damascene feature on a substrate, other features, such as vias, lines, contacts, and other features known in the art, may be formed by the processes described herein.

Figure 2 is a flow chart illustrating steps of one embodiment of the invention in forming a dual damascene structure. The flow chart is provided for illustrative purposes and

should not be construed as limiting the scope of the invention. A dielectric liner/barrier layer is typically first deposited upon the substrate surface to prevent diffusion of subsequently deposited material, such as copper, into the substrate at step 300. The dielectric liner/barrier layer preferably comprises a low k material and can perform as an etch stop to protect the substrate during etching and removal of subsequently deposited layers.

A feature definition is then formed on the dielectric liner/barrier layer at step 310. The feature definition is generally formed by depositing dielectric material on the barrier layer and etching the definition therein. The deposited dielectric material may be deposited in one or more layers of dielectric material with one or more etch stop or barrier layers of dielectric material disposed therein to help form and define the dual damascene definition. The dual damascene definition is etched in the dielectric material by conventional means and processes known in the art and may be performed in one or more steps. For example, to form a dual damascene definition, the dielectric material can be etched to form vertical interconnects, such as vias/contacts, and then etched to form horizontal interconnects, such as lines/trenches. Alternatively, both horizontal and vertical interconnects may be formed in a single etching process.

One process for forming a dual damascene definition is a "self-aligning contact" (SAC) scheme in which an etch stop layer of a dielectric material is deposited on a first dielectric layer and etched to define vertical interconnects, such as vias/contacts, and to expose the underlying first dielectric layer before a second dielectric layer is deposited. The vertical and horizontal interconnects are then etched in a single step in the first and second dielectric layers to form the dual damascene definition. Alternatively, in a "counter-bore" scheme, a series of dielectric layers are deposited on a substrate. Then vertical interconnects such as vias/contacts are etched through all of the layers and horizontal interconnects such as lines/trenches are etched through the top layers. In the alternative, the lines/trenches are etched in the top layers and then the vias/contacts are etched through the bottom layers.

A conductive barrier layer is then deposited on the substrate surface and on the exposed surfaces of the dual damascene definition at step 320. The conductive barrier layer is deposited to prevent diffusion of subsequently deposited materials, such as copper, into the surrounding dielectric material and to provide adhesion between the subsequently deposited materials and the substrate. The conductive barrier layer is conformally deposited

over the surfaces of the dual damascene definition and may be deposited by a chemical vapor deposition (CVD) technique, a physical deposition (PVD) technique, such as ionized metal plasma (IMP) PVD, or any other process conventionally known in the art.

Thereafter, a layer of conductive material is deposited on the conductive barrier layer to fill at least a portion of the dual damascene definition at step 330. The conductive material is deposited using either a CVD technique, a PVD technique, such as ionized metal plasma (IMP) PVD, an electrochemical deposition technique, such as electroplating, or other means known in the art to fill at least a portion of the definition to form the conductive structure.

After the conductive material has been deposited, the substrate surface is planarized at step 340 using chemical mechanical polishing or other planarizing methods known in the art to expose the underlying dielectric material and form the dual damascene structures.

After planarizing the substrate surface, at least a portion of the deposited dielectric material is removed from the surface of the substrate at step 350. Substantially all of the dielectric material between dual damascene structures or the dielectric material surrounding a dual damascene structure may be removed to the low k barrier layer. Alternatively, a portion of the dielectric material between dual damascene structures or surrounding a dual damascene structure is removed, such as the dielectric material adjacent the horizontal interconnects of the dual damascene structures. The dielectric material may be removed by a etching means or process known in the art and may be performed in one or more steps. Additionally, the invention contemplates removal of the dielectric material by other processes suitable for removing dielectric materials known in the art, such as chemical mechanical polishing.

A low k dielectric barrier may be optionally deposited on the substrate surface at step 360 to prevent conductive material from diffusing into subsequently deposited materials.

A low k dielectric material is deposited in a gap fill process on the substrate surface at step 370. Generally, the low k gap fill is deposited to sufficient depth to cover the remaining dual damascene structures formed on the substrate surface. The low k gap fill layer can then be planarized to expose the dual damascene structure.

Alternatively, a second dielectric material may be deposited on the low k dielectric material at step 380 for formation of subsequent semiconductor devices and structures

including additional dual damascene definitions. The second dielectric material preferably comprises a self-planarizing material, such as a self-planarizing oxide layer. A second dual damascene definition may then be etched into the planarized second dielectric material and portions of the low k dielectric material. The dual damascene definition is preferably etched and filled at step 390 in the same or similar manner as described above in steps 310 to 340

Figures 3A through 3H further illustrate the process of one embodiment of the invention described herein. Referring to Figure 3A to 3H, generally, an aperture 406, such as a dual damascene definition, is formed in dielectric material 404 deposited on a substrate barrier layer 402. The substrate barrier layer 402 is preferably a low k dielectric material conformally deposited on the substrate 400 to prevent interlayer diffusion of materials into the substrate 400. The aperture 406 may be etched by means conventionally known in the art in the dielectric material 404. Optionally, the substrate may then be exposed to a reactive pre-clean process to remove contaminants, particulate matter, and oxides that may have formed on the exposed portions of the aperture. A conductive barrier layer 408 is deposited on exposed surfaces of the aperture 406, and a conductive material 410 is subsequently deposited on the conductive barrier layer 408. The substrate 400 may then be planarized using a chemical mechanical polishing process to form a feature 413 thereon.

At least a portion of the dielectric material 404 is then removed from the substrate 400. A low k barrier layer 412 is conformally deposited over the feature 413 and substrate barrier layer 402. During the dielectric removal process, the low k barrier layer 402 acts as an etch stop on the substrate surface during removal of the dielectric layer 404. A low k gap fill layer 414 is deposited over the feature 413, with the low k gap fill 414 deposited to at least substantially cover the feature 413. A planarizing dielectric layer 416 is then deposited on the low k gap fill 414. The dielectric layers 414 and 416 are then etched as aperture 404 to form apertures 418. A barrier layer 420 and conductive material 422 are then deposited respectively in aperture 418 and planarized to expose the underlying dielectric layer 404 and to form feature 423.

Referring to Figure 3A, the aperture 406 is formed by depositing and pattern etching one or more dielectric layers 404 on the low k barrier layer 402 conformally deposited on the substrate 400. The term aperture is broadly defined in accordance with its customary usage in the semiconductor industry and is more particularly defined herein as a definition of a substrate structure formed in a substrate material or materials deposited on a substrate,

and includes, but is not limited to, such substrate structures as trench, lines, vias, contact, interconnects and dual damascenes. As shown in Figure 3A, the aperture 406 is a dual damascene definition.

Substrate 400 comprises a doped silicon substrate or material such as glass, thermal oxide, quartz or other materials conventionally used in semiconductor fabrication. The substrate 400 may also comprise a pattern substrate having dielectric layers and conductive layers, such as conductive lines 401, which can include a series of underlined layers interconnects with various materials. The substrate barrier layer 402 comprises a low k material, such as silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide (BLOk™), or other low k material known in the art. Preferably silicon nitride or amorphous hydrogenated silicon carbide is used as the substrate barrier layer 402. The amorphous hydrogenated silicon carbide (BLOk™) and process for deposition such materials is more fully described in co-pending U.S. Patent Application Serial No. 09/165,248, entitled, "A Silicon Carbide Deposition For Use As A Barrier Layer and An Etch Stop," filed on October 1, 1998, and incorporated herein by reference to the extent not inconsistent with the invention. The substrate barrier layer 402 can also act as an etch stop to protect the substrate during etching and removal of subsequent layers that may be deposited thereon.

The dielectric layer 404 may be of any dielectric material whether presently known or yet to be discovered as within the scope of the invention known in the art. The dielectric material may be deposited by conventional methods known in the art, such as by chemical vapor deposition (CVD) techniques. The dielectric layer preferably comprises silicon oxide deposited by a plasma enhanced chemical vapor deposition (PECVD) process, such as the plasma enhanced deposition of silane or tetraethylorthosililate (TEOS), in the DxZ™ CVD processing chamber described above.

An exemplary processing regime for depositing a silicon dioxide film is as follows. The silicon dioxide layer is deposited by introducing a silane gas at a flow rate between about 20 sccm and about 400 sccm, introducing nitrous oxide at a flow rate between about 500 sccm and about 4,000 sccm into the processing chamber, and generating a plasma by supplying a power level between about 100 watts and about 1000 watts to a gas distribution manifold to deposit the silicon nitride film.

During the deposition process, the processing chamber is maintained at a pressure

of about 0.1 Torr or greater, and the substrate is maintained at a temperature of about 450°C or below. The processing chamber is preferably maintained at a pressure between about 0.1 Torr and about 12 Torr. The substrate is preferably maintained at a temperature between about 200°C and about 450°C. The gas distribution manifold is generally spaced from the substrate by a distance between about 200 mils and about 800 mils (thousandths of an inch), or a distance between about 5 mm and about 20 mm.

The dielectric layer 404 may then be etched with any dielectric etching or polishing process known in the art including plasma etching. An example of etching dielectric materials, such as silicon oxide, is more fully described in U.S. Patent No. 5,843,847, entitled "Method for Etching Dielectric layers with High selectivity and Low Microloading," issued on December 1, 1998, which is assigned to Applied Materials, Inc., and incorporated herein by reference to the extent not inconsistent with the invention.

While not shown, in etching and forming the dual damascene aperture 406, the dielectric layer 404 may comprise multiple layers and further comprise interlayer barrier layers and etch stops disposed therein to help define the aperture 406 formed during the etch process. For example, a first dielectric layer, such as silicon oxide, is deposited on the substrate surface, an etch stop layer of a dielectric material, such as silicon nitride, silicon oxycarbide, or amorphous hydrogenated silicon carbide is deposited on a first dielectric layer and etched to define vertical interconnects, such as vias/contacts, and to expose the underlying first dielectric layer before a second dielectric layer, such as silicon oxide, is deposited. The vertical and horizontal interconnects are then etched in a single step in the first and second dielectric layers to form the aperture 406. The interconnects may be etched through the liner/barrier layer 402 in order to contact underlying metal lines 401.

Optionally, the substrate may then be exposed to a reactive pre-clean process to remove some oxides and other contaminants, such as etch residue and metal contaminants, in the aperture 406 and on the surface of the substrate, which may interfere with subsequent layer deposition. The reactive pre-clean process comprises exposing the substrate surface to a plasma, preferably comprising hydrogen and/or an inert gas, such as argon, at a power density between of 0.03 watts/cm^2 and about 3.2 watts/cm^2, or at a power level between about 10 watts and 1000 for a 200 millimeter substrate. The processing chamber is maintained at a pressure of about 20 Torr or less and at a substrate temperature of about 450C or less during the reactive clean process. The reactive pre-clean described herein can

be used to remove oxides formed on metal layers, such as the conductive barrier layers described herein or for copper. The invention contemplates the use of other oxide removal processes, such as nitrogen reduction of oxide formations on metal layers.

Referring to Figure 3B, the conductive barrier layer 408 is deposited on the exposed surface of the aperture 406 formed in dielectric layer 404. The conductive barrier layer 408 is deposited upon the exposed surfaces of the aperture 406 to prevent interlayer diffusion, such as copper migration into the surrounding dielectric material, and to improve adhesion layer between the dielectric material 404 and subsequently deposited metal layers. The conductive barrier layer 408 may be formed by the disassociation of an organometallic precursor by a thermal or plasma enhanced chemical vapor deposition process, or alternatively, deposited by a physical vapor deposition process, such as an ionized metal plasma physical vapor deposition process (IMP-PVD). Preferably, the conductive barrier layer 408 comprises materials selected from the group of titanium, titanium nitride, titanium silicon nitride, tungsten nitride, tungsten silicon nitride, tantalum, tantalum nitride, tantalum silicon nitride, and refractory metals such as niobium, vanadium, and nitrides thereof, and combinations thereof.

Referring to Figure 3C, conductive material 410 is deposited on the conductive barrier layer 408. The conductive material 410 is deposited to fill the at least a portion of the aperture 406, and is preferably deposited to fill the aperture 406. Alternatively, the conductive material 410 comprises a seed layer of a conducting metal to fill at least a portion of the aperture 406 and a subsequent metal fill layer on the seed layer.

The conductive material 410 preferably comprises copper or aluminum. The conductive material 410 may be doped with material, such as phosphorous and boron, to improve deposition and fill of the aperture 406. The conductive material 410 may be deposited by a chemical vapor deposition (CVD) technique, a physical deposition (PVD) technique, such as ionized metal plasma (IMP) PVD, electroplating, electroless deposition, evaporation deposition, or any other process conventionally known in the art.

Preferably, the metal layer 410 comprises copper and is deposited using an electroplating technique. An exemplary electroplating method is describing co-pending U.S. Patent Application Serial No. 09/114,865, filed on July 13, 1998, and is incorporated herein by reference to the extent not inconsistent with the invention.

The conductive material 410 may also be deposited by a combination of processing

regimes. For example, a seed layer may be deposited by chemical vapor deposition and PVD layer may be deposited on top of a CVD metal seed layer, and the PVD metal layer may be deposited at a temperature less than the melting temperature of the material of the conducting metal being deposited which allows reflow of the seed layer and the conducting metal layer to fill the aperture therein. After the conductive material 410 is deposited, the substrate may be annealed to recrystallize the conductive material and remove any voids formed in the aperture 406.

Referring back to Figure 3C, the aperture 406 may be further processed by planarizing the top portion of the aperture 406 preferably by a chemical mechanical polishing process. During the planarization process portions of the conducting metal layer 410 and the dielectric layer 404 are removed from the top of the structure leaving a planar surface with a conducting feature 413 formed therein.

Referring to Figure 3D, the remaining dielectric material 404 from the aperture etching process is then etched and removed from the substrate surface. A suitable process for removing the remaining dielectric material 404 is more fully described in U.S. Patent No. 5,843,847, entitled "Method for Etching Dielectric layers with High selectivity and Low Microloading," issued on December 1, 1998, which is assigned to Applied Materials, Inc., and incorporated herein by reference to the extent not inconsistent with the invention. The dual damascene structures formed 413 in the dielectric material 404 acts as a hardmask during the etch process, which allows some dielectric material 404 to be retained in the space located between the substrate and the trench level of the dual damascene structure which surrounds the lower or via portion of the dual damascene structure. The retained dielectric material can act as a diffusion barrier to the conductive material and further insolates subsequently deposited low k material from the conductive material.

Referring to Figure 3E, a low k barrier layer 412 may be deposited conformally over the feature 413 and on the substrate 402 to prevent diffusion of the conductive material into the surrounding material. The low k dielectric barrier may comprise silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide (BLOk™), and combinations thereof, and preferably silicon nitride or amorphous hydrogenated silicon carbide are used.

Referring to Figure 3F a low k gap fill dielectric material 414 may be deposited into the dual damascene structures 413 typically covering the surfaces of the dual damascene structures 413. The low k dielectric material 414 preferably comprises a silicon and carbon

containing material, such as silicon oxycarbide, but may comprise silicon carbide, undoped silicon dioxide, also known as undoped silicon glass (USG), fluorine doped silicon glass, (FSG) or other low k dielectric material.

One exemplary processing regime for depositing a low k silicon and carbon containing material as a gap fill comprises introducing a processing gas including trimethylsilane to a processing chamber at a flow rate between about 50 sccm and about 100 sccm, preferably about 175 sccm, introducing an oxidizing gas, such as a mixture of oxygen and between about 6 wt% and about 18 wt% ozone, at a flow rate between about 2500 sccm and about 10000 sccm, preferably at about 5000 sccm, introducing an inert gas, such as helium into the processing chamber at a rate between about 1000 sccm and about 10000 sccm, preferably at about 8000 sccm, maintaining a chamber pressure between about 50 Torr and about 250 Torr, preferably at about 100 Torr, and maintaining a substrate surface temperature between about 50°C and about 250°C, preferably at about 125°C. The gas distribution plate 11 is spaced between about 180 mils and about 500 mils, preferably at about 210 mils, from the substrate.

Another exemplary low k dielectric material that may be used as a gap fill is a silicon oxide film containing silicon-carbon bonds deposited from organosilane and organosiloxane precursors in a plasma-enhanced CVD process and is disclosed in U.S. Patent No. 6,054,379, entitled "Method of Depositing a Low K Dielectric With Organosilane," issued on April 25, 2000 and in co-pending U.S. Patent Application Serial No. 09/247,381, entitled "Plasma Process For Depositing Dielectric Constant Films," filed on February 10, 1999, both of which are assigned to Applied Materials, Inc., and is incorporated herein by reference to the extent not inconsistent with the invention.

Referring to Figure 3G a self planarizing dielectric material 416 is deposited upon the low k dielectric material 414. The second dielectric material preferably comprises a self-planarizing PECVD silicon oxide layer such as spin-on polymers or oxides deposited in liquid form, such as by the reaction silane and hydrogen peroxide. The self-planarizing low k dielectric layer is preferably an oxide layer deposited by plasma enhanced chemical vapor deposition. An example of such a planarizing layer is disclosed in co-pending U.S. Patent Application Serial No. 09/247,381, entitled "Plasma Process For Depositing Dielectric Constant Films," filed on February 10, 1999, assigned to Applied Materials, Inc., and is incorporated herein by reference to the extent not inconsistent with the invention.

Referring to Figure 3H, a second aperture 418 may be etched in the low k dielectric material 414, the self-planarizing dielectric material 416, and the low k barrier layer 412. The aperture 418 may be formed by the methods used to form the aperture 406. An example of etching a low k dielectric material is described in co-pending U.S. Patent Application Serial No. 09/329,012, entitled, "Integrated Low K Dielectrics And Etch Stops," filed on June 9, 1999, and incorporated herein by reference to the extent not inconsistent with the invention.

After the aperture 418 is formed in the dielectric materials, a barrier layer 420 and a conducting metal layer 422, such as copper, are deposited sequentially in the aperture 418 to form a second feature 423 connected to feature 413. Following fill of the aperture 418, the dual damascene structure is planarized and then annealed to recrystallized the copper forming part of the dual damascene structure. Other subsequent processing of the substrate 400 may be performed including additional deposition of layers etching for a new and substrate of the process on integrated circuit (IC) manufacturing including repetition the process step in the invention described herein.

It is contemplated that removing a silicon oxide layer and then depositing a low k dielectric gap fill layer on a dual damascene structure, low k dual damascene structures with minimized interlayer diffusion can be formed without a chemical mechanical polishing step and without breaking the seal on a vacuum. Eliminating or minimized chemical polishing of the low k dielectric material minimizes the distortion of deposited materials and layers and possible delamination of the low k dielectric material. Without the need to break the vacuum seal, exposure of the substrate to contaminants, such as moisture and oxygen, which can detrimentally affect the dielectric constant and device performance, is minimized.

Further, it is believed that the low k gap fill will allow lower intralevel and interlevel dielectric constants since the use of etch stops or barrier layers, such as silicon nitride, which can detrimentally affect the dielectric constant of the material surrounding the dual damascene, is minimized. Additionally, it is believed that by forming the dual damascene structures in a harder material such as the silicon oxide compared to the low k gap-fill material, dual damascene structures with improved hardness and lower deformation and mechanical stresses can be formed.

While foregoing is directed to the preferred embodiment of the present invention,

other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is Claimed is:

1. A method for processing a substrate, comprising:

(a) forming a feature definition in a dielectric material deposited on a surface of a substrate;

(b) depositing one or more conductive materials to fill at least a portion of the feature definition;

(c) planarizing the substrate surface to expose the dielectric material;

(d) removing at least a portion of the dielectric material; and

(e) depositing a low k dielectric material.

2. The method of claim 1, wherein forming a feature definition in a dielectric material comprises:

(a) depositing a first dielectric material;

(b) depositing a second dielectric material on the first dielectric material;

(c) depositing a third dielectric layer on the second dielectric material;

(d) etching the first and second dielectric layers to form a vertical interconnect; and

(e) etching the third dielectric layer to form a horizontal interconnect.

3. The method of claim 2, wherein the first and third dielectric layers comprises silicon oxide.

4. The method of claim 2, wherein the second dielectric layer is an etch stop.

5. The method of claim 4, wherein the second dielectric layer comprise silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

6. The method of claim 1, wherein forming a feature definition in a dielectric material comprises:

(a) depositing a first dielectric material;

(b) depositing a second dielectric material on the first dielectric material;

(c) etching the second dielectric layer to exposed a portion of the first dielectric layer;

(d) depositing a third dielectric layer on the second dielectric material and exposed portion of the first dielectric layer; and

(e) etching the first and third dielectric layers to form a vertical interconnect and to form a horizontal interconnect.

7. The method of claim 2, wherein the first and third dielectric layers comprises silicon oxide.

8. The method of claim 2, wherein the second dielectric layer is an etch stop.

9. The method of claim 4, wherein the second dielectric layer comprise silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

10. The method of claim 1, further comprising depositing a low k barrier layer on the surface of the substrate prior to depositing the dielectric material.

11. The method of claim 10, wherein the low k barrier layer deposited on the surface of the substrate comprises a low k material selected from the group of silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

12. The method of claim 1, wherein depositing the one or more conductive materials comprises depositing a conductive barrier layer of a first conductive material and then depositing a second conductive material on the conductive barrier layer.

13. The method of claim 12, wherein the first conductive material and the second conductive material are deposited by chemical vapor deposition, physical vapor deposition, or a electrochemical deposition technique.

14. The method of claim 12, wherein the first conductive material comprises one or more materials selected from the group of titanium, titanium nitride, titanium silicon nitride,

tungsten, tungsten nitride, tungsten silicon nitride, tantalum, tantalum nitride, tantalum silicon nitride, and combinations thereof.

15. The method of claim 12, wherein the second conductive material is selected from the group of copper, doped copper, aluminum, doped aluminum, and combinations thereof.

16. The method of claim 1, wherein the low k dielectric material comprises a silicon and carbon containing material.

17. The method of claim 16, wherein the low k dielectric material has a dielectric constant of about 4.0 or less.

18. The method of claim 1, further comprising depositing a low k barrier layer prior to depositing the low k dielectric material.

19. The method of claim 18, wherein the low k barrier layer deposited prior to depositing the low k dielectric material comprises a low k material selected from the group of silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

20. The method of claim 1, wherein planarizing the substrate surface comprises chemical mechanical polishing the substrate surface.

21. The method of claim 1, further comprising planarizing the substrate surface after depositing the low k dielectric layer.

22. The method of claim 1, wherein removing at least a portion of the dielectric material comprises etching or polishing substantially all the dielectric material to the substrate surface.

23. The method of claim 2, wherein removing at least a portion of the dielectric material comprises etching or polishing the dielectric material adjacent the horizontal interconnect.

24. The method of claim 6, wherein removing at least a portion of the dielectric material comprises etching or polishing the dielectric material adjacent the horizontal interconnect.

25. A method for forming a dual damascene interconnect, comprising:

(a) depositing one or more dielectric layers on a substrate;

(b) etching the one or more dielectric layers to form a dual damascene definition therein, the dual damascene definition having a vertical interconnect and a horizontal interconnect;

(c) depositing a conductive barrier layer over exposed surfaces of the dual damascene definition;

(d) depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition;

(e) planarizing the filled dual damascene definition to expose the one or more dielectric layers;

(f) removing at least a portion of the one or more dielectric layers;

(g) depositing a low k dielectric material; and

(h) depositing a self-planarizing dielectric layer on the low k dielectric material.

26. The method of claim 25, further comprising etching the low k dielectric material and the self-planarizing dielectric layer to form a dual damascene definition.

27. The method of claim 26, further comprising repeating steps (c) through (e).

28. The method of claim 25, wherein the one or more dielectric layers comprise silicon oxide, silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

29. The method of claim 25, wherein the conductive barrier layer comprises a material selected from the group of titanium, titanium nitride, titanium silicon nitride, tungsten, tungsten nitride, tungsten silicon nitride, tantalum, tantalum nitride, tantalum silicon nitride, and combinations thereof.

30. The method of claim 25, wherein the conductive material is selected from the group of copper, doped copper, aluminum, doped aluminum, and combinations thereof.

31. The method of claim 25, wherein the low k dielectric material comprises a silicon and carbon containing material.

32. The method of claim 31, wherein the low k dielectric material has a dielectric constant of about 4.0 or less.

33. The method of claim 25, wherein removing at least a portion of the dielectric material comprises etching or polishing substantially all the dielectric material to the substrate surface.

34. The method of claim 25, wherein removing at least a portion of the dielectric material comprises etching or polishing the dielectric material adjacent the horizontal interconnect.

35. The method of claim 25, further comprising depositing a low k barrier layer prior to depositing the dielectric material.

36. The method of claim 35, wherein the low k barrier layer deposited on the surface of the substrate comprises a low k material selected from the group of silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

37. The method of claim 25, further comprising depositing a low k barrier layer prior to depositing a low k dielectric material.

38. The method of claim 37, wherein the low k barrier layer deposited prior to depositing the low k dielectric material comprises a low k material selected from the group of silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

39. The method of claim 25, wherein etching the one or more dielectric layers comprises etching the first and second dielectric layers to form a vertical interconnect and etching the third dielectric layer to form a horizontal interconnect.

40. The method of claim 25, further comprising performing a chemical mechanical polishing process on the substrate.

41. A method for forming a dual damascene interconnect, comprising:

(a) depositing a first dielectric material;

(b) depositing a second dielectric material on the first dielectric material;

(c) etching the second dielectric layer to exposed a portion of the first dielectric layer;

(d) depositing a third dielectric layer on the second dielectric material and exposed portion of the first dielectric layer;

(e) etching the first and third dielectric layers to form a vertical interconnect and a horizontal interconnect of a dual damascene definition;

(f) depositing a conductive barrier layer over exposed surfaces of the dual damascene definition;

(g) depositing a conductive material over the conductive barrier layer to fill at least a portion of the dual damascene definition;

(h) planarizing the filled dual damascene definition to expose the one or more dielectric layers;

(i) removing the one or more dielectric layers;

(j) depositing a low k dielectric material on the substrate; and

(k) depositing a self-planarizing dielectric layer on the low k dielectric material.

42. The method of claim 41, further comprising etching the low k dielectric material and the self-planarizing dielectric layer to form a dual damascene definition.

43. The method of claim 41, further comprising repeating steps (f) through (h).

44. The method of claim 41, wherein the first and third dielectric layers comprises

silicon oxide.

45. The method of claim 41, wherein the second dielectric layer is an etch stop.

46. The method of claim 41, wherein the second dielectric layer comprise silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

47. The method of claim 41, wherein removing at least a portion of the dielectric material comprises etching or polishing substantially all the dielectric material to the substrate surface.

48. The method of claim 41, wherein removing at least a portion of the dielectric material comprises etching or polishing the dielectric material adjacent the horizontal interconnect.

49. The method of claim 41, wherein the conductive barrier layer comprises a material selected from the group of titanium, titanium nitride, titanium silicon nitride, tungsten, tungsten nitride, tungsten silicon nitride, tantalum, tantalum nitride, tantalum silicon nitride, and combinations thereof.

50. The method of claim 41, wherein the conductive material is selected from the group of copper, doped copper, aluminum, doped aluminum, and combinations thereof.

51. The method of claim 41, wherein the low k dielectric material comprises a silicon and carbon containing material.

52. The method of claim 41, wherein the low k dielectric material has a dielectric constant of about 4.0 or less.

53. The method of claim 41, further comprising depositing a low k barrier layer prior to depositing a low k dielectric material.

54. The method of claim 53, wherein the low k barrier layer deposited prior to depositing the low k dielectric material comprises a low k material selected from the group of silicon nitride, silicon oxycarbide, amorphous hydrogenated silicon carbide, and combinations thereof.

55. The method of claim 1, wherein depositing the low k dielectric material comprises introducing a processing gas including trimethylsilane to a processing chamber at a flow rate between about 50 sccm and about 1000 sccm, introducing an oxidizing gas at a flow rate between about 2500 sccm and about 10000 sccm, introducing an inert gas into the processing chamber at a rate between about 1000 sccm and about 10000 sccm, maintaining a chamber pressure between about 50 Torr and about 200 Torr, and maintaining a substrate surface temperature between about 50°C and about 250°C.

56. The method of claim 1, wherein depositing the low k dielectric material comprises introducing a processing gas including trimethylsilane to a processing chamber at a flow rate of about 175 sccm, introducing an oxidizing gas at a flow rate of about 5000 sccm, introducing an inert gas into the processing chamber at a rate of about 8000 sccm, maintaining a chamber pressure of about 100 Torr, and maintaining a substrate surface temperature of about 125°C.

57. The method of claim 25, wherein depositing the low k dielectric material comprises introducing a processing gas including trimethylsilane to a processing chamber at a flow rate between about 50 sccm and about 1000 sccm, introducing an oxidizing gas at a flow rate between about 2500 sccm and about 10000 sccm, introducing an inert gas into the processing chamber at a rate between about 1000 sccm and about 10000 sccm, maintaining a chamber pressure between about 50 Torr and about 200 Torr, and maintaining a substrate surface temperature between about 50°C and about 250°C.

58. The method of claim 25, wherein depositing the low k dielectric material comprises introducing a processing gas including trimethylsilane to a processing chamber at a flow rate of about 175 sccm, introducing an oxidizing gas at a flow rate of about 5000 sccm, introducing an inert gas into the processing chamber at a rate of about 8000 sccm,

maintaining a chamber pressure of about 100 Torr, and maintaining a substrate surface temperature of about 125°C.

59. The method of claim 41, wherein depositing the low k dielectric material comprises introducing a processing gas including trimethylsilane to a processing chamber at a flow rate between about 50 sccm and about 1000 sccm, introducing an oxidizing gas at a flow rate between about 2500 sccm and about 10000 sccm, introducing an inert gas into the processing chamber at a rate between about 1000 sccm and about 10000 sccm, maintaining a chamber pressure between about 50 Torr and about 200 Torr, and maintaining a substrate surface temperature between about 50°C and about 250°C.

60. The method of claim 41, wherein depositing the low k dielectric material comprises introducing a processing gas including trimethylsilane to a processing chamber at a flow rate of about 175 sccm, introducing an oxidizing gas at a flow rate of about 5000 sccm, introducing an inert gas into the processing chamber at a rate of about 8000 sccm, maintaining a chamber pressure of about 100 Torr, and maintaining a substrate surface temperature of about 125°C.

ABSTRACT OF THE DISCLOSURE

A method and apparatus for processing a substrate to form a feature in low k dielectric materials. One aspect of the invention provides a method for processing a substrate including forming a feature definition in a dielectric material deposited on a surface of a substrate, depositing one or more conductive materials to fill at least a portion of the feature definition, planarizing the substrate surface to expose the dielectric material, removing at least a portion of the dielectric material, and depositing a low k dielectric material.

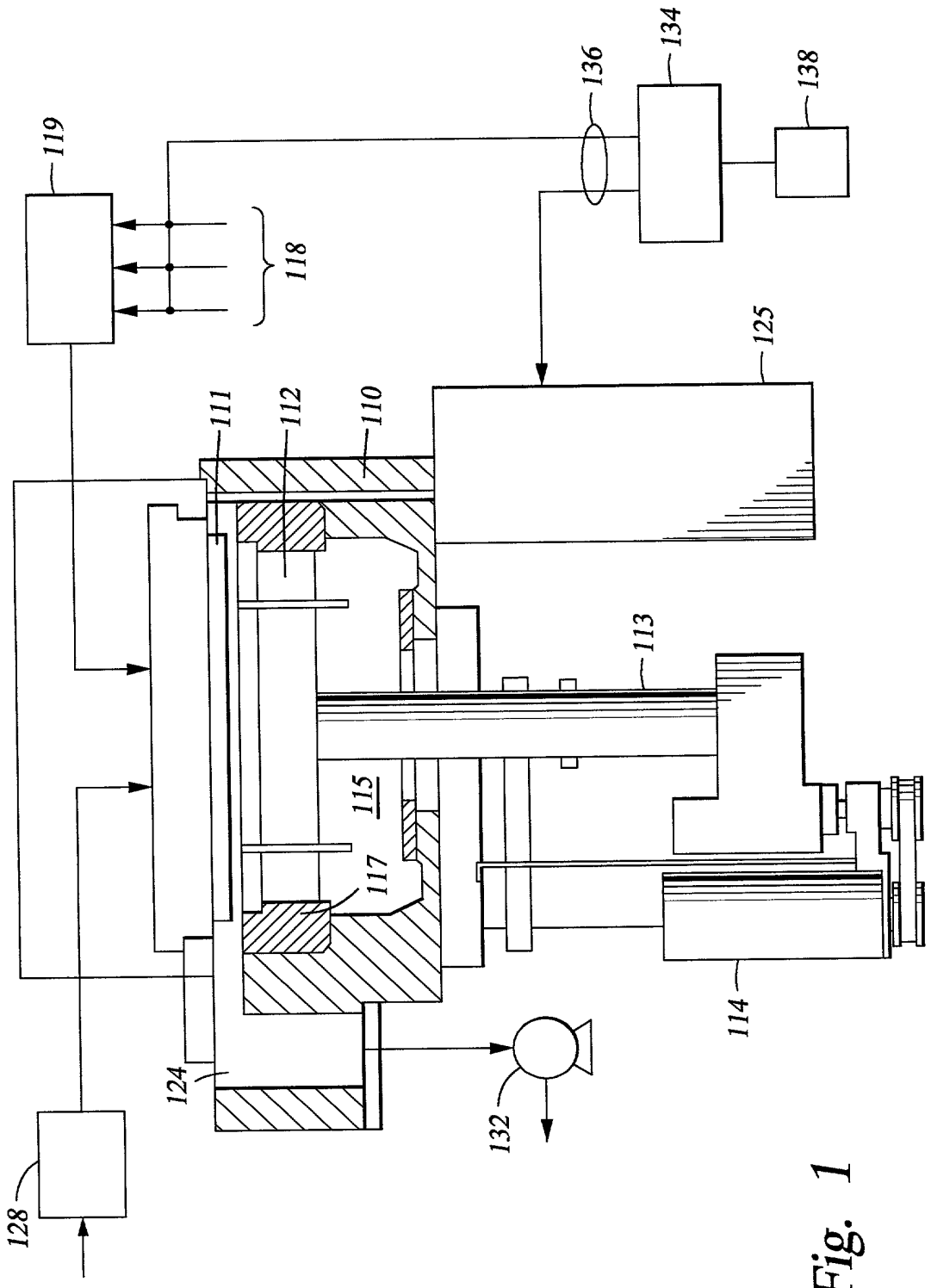
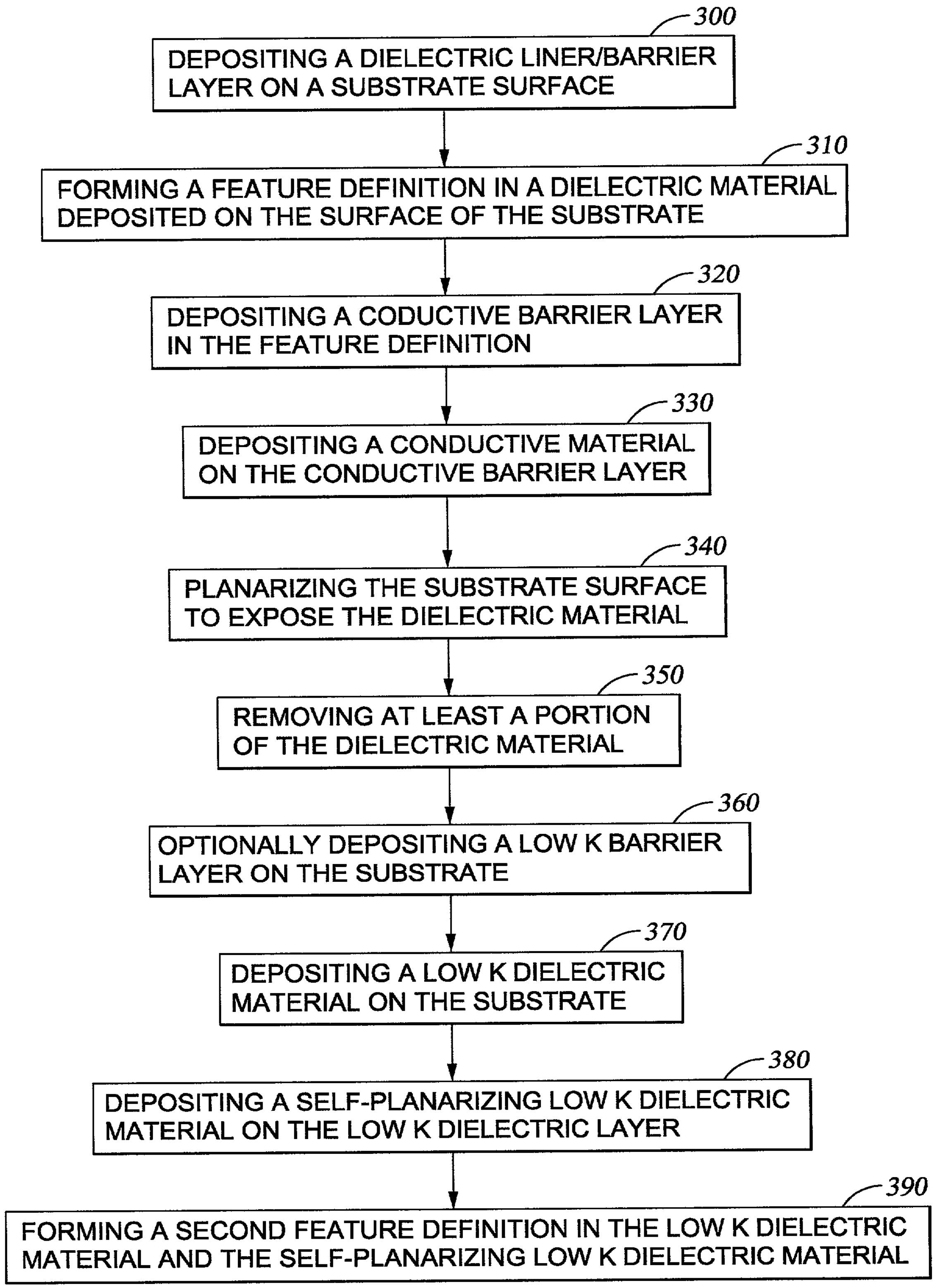


Fig. 1


300
DEPOSITING A DIELECTRIC LINER/BARRIER LAYER ON A SUBSTRATE SURFACE
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FORMING A FEATURE DEFINITION IN A DIELECTRIC MATERIAL DEPOSITED ON THE SURFACE OF THE SUBSTRATE
320
DEPOSITING A CODUCTIVE BARRIER LAYER IN THE FEATURE DEFINITION
330
DEPOSITING A CONDUCTIVE MATERIAL ON THE CONDUCTIVE BARRIER LAYER
340
PLANARIZING THE SUBSTRATE SURFACE TO EXPOSE THE DIELECTRIC MATERIAL
350
REMOVING AT LEAST A PORTION OF THE DIELECTRIC MATERIAL
360
OPTIONALLY DEPOSITING A LOW K BARRIER LAYER ON THE SUBSTRATE
370
DEPOSITING A LOW K DIELECTRIC MATERIAL ON THE SUBSTRATE
380
DEPOSITING A SELF-PLANARIZING LOW K DIELECTRIC MATERIAL ON THE LOW K DIELECTRIC LAYER
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FORMING A SECOND FEATURE DEFINITION IN THE LOW K DIELECTRIC MATERIAL AND THE SELF-PLANARIZING LOW K DIELECTRIC MATERIAL

Fig. 2

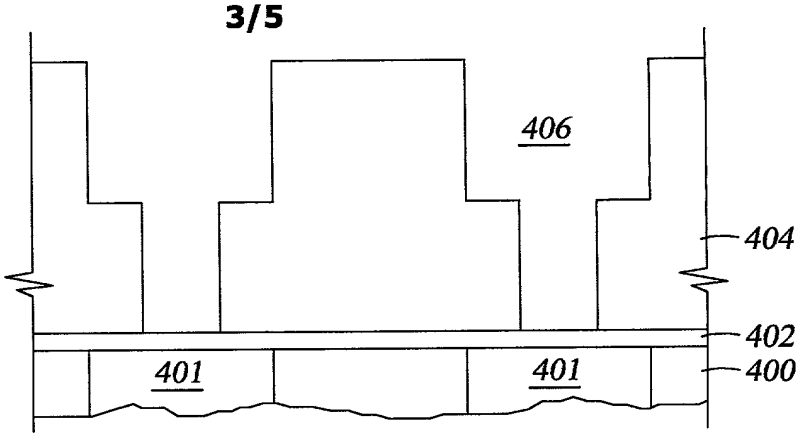


Fig. 3A

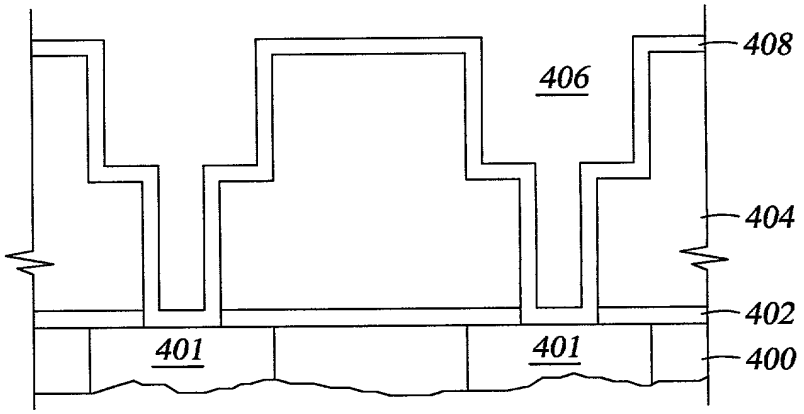


Fig. 3B

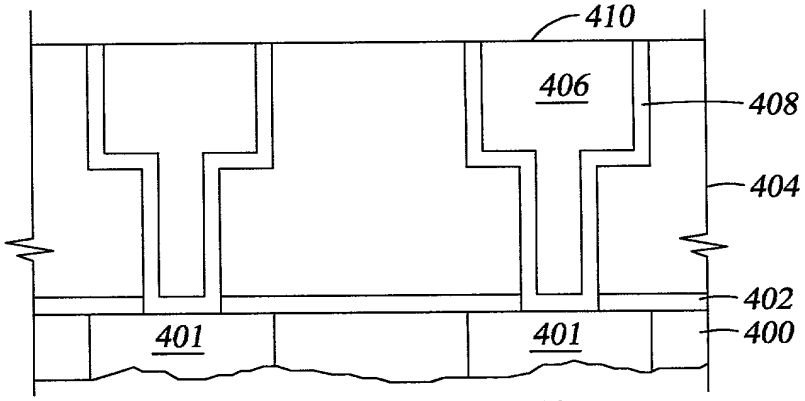


Fig. 3C

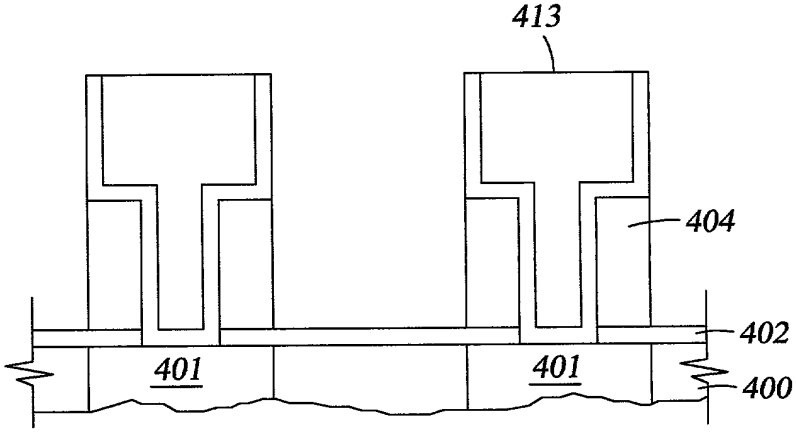


Fig. 3D

Fig. 3E

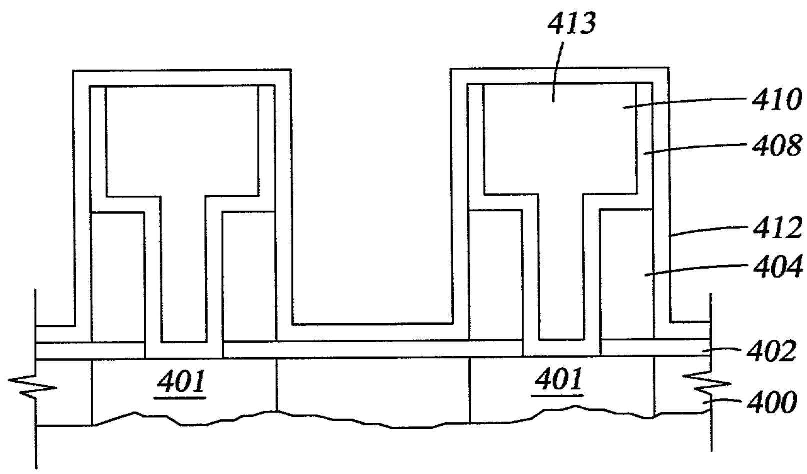


Fig. 3F

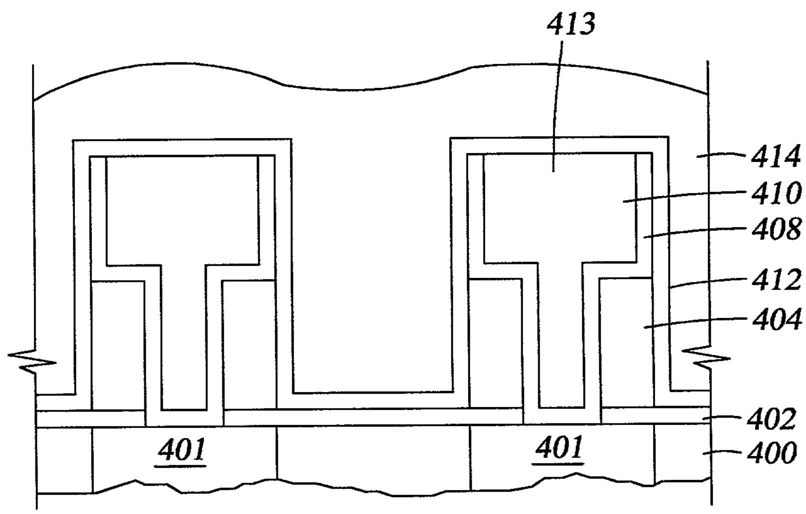
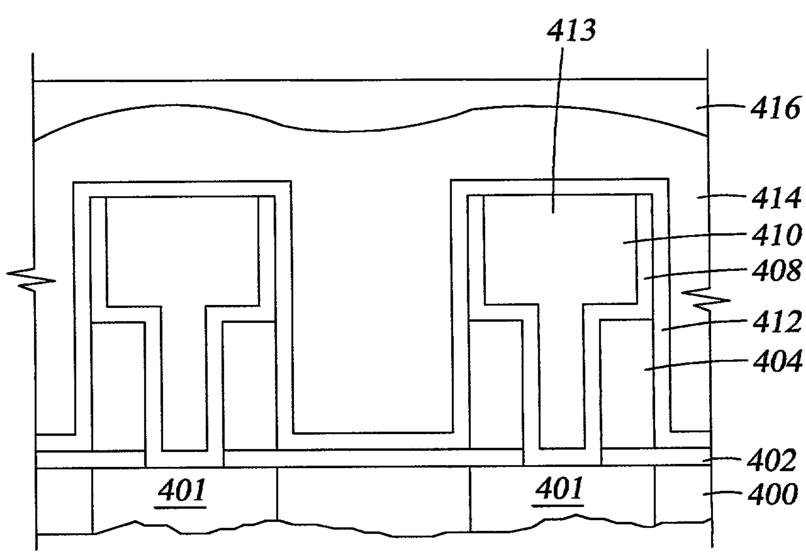


Fig. 3G



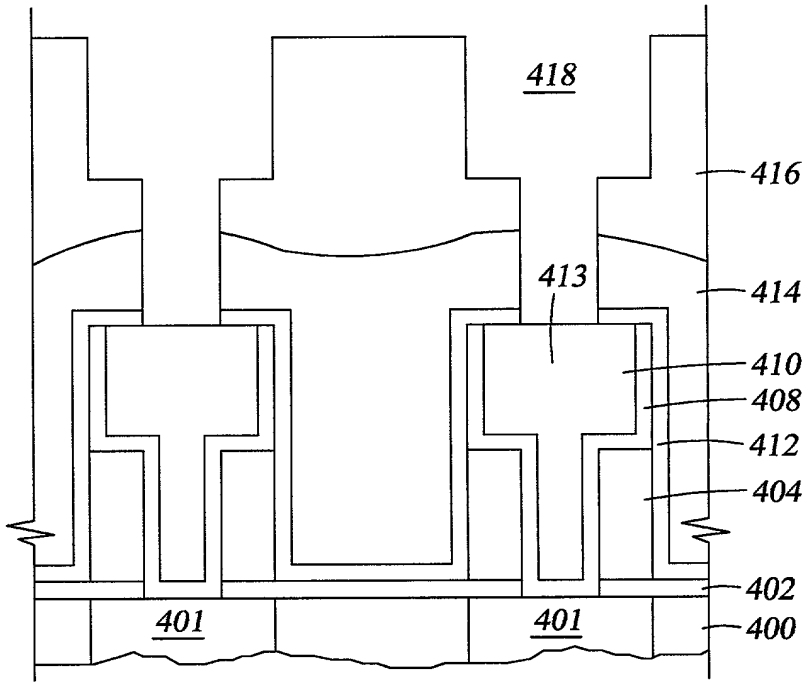

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Fig. 3H

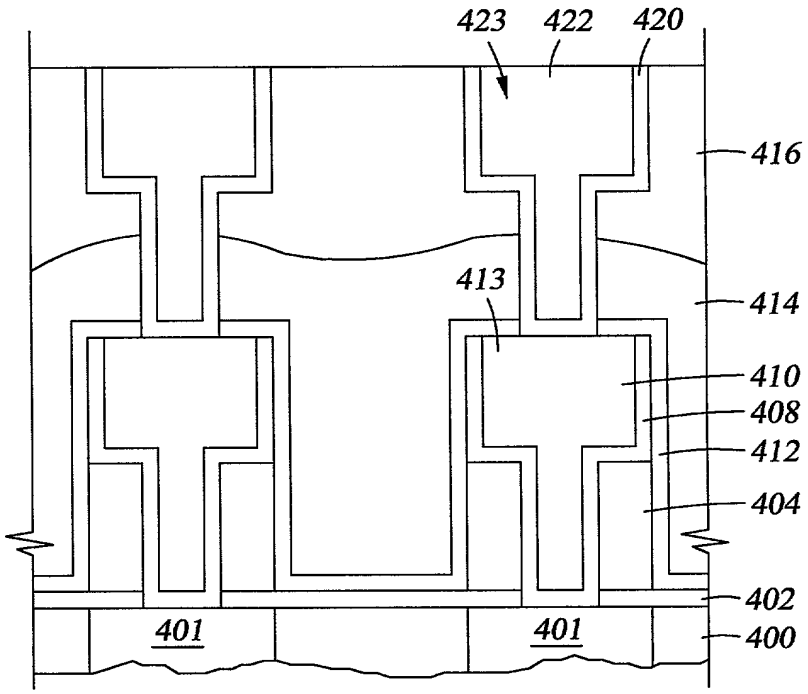
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Fig. 3I

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

This declaration is of the following type:

[X] original
[ ] divisional
[ ] continuation
[ ] continuation-in-part

INVENTORSHIP IDENTIFICATION

My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

NOVEL INTEGRATION SCHEME FOR DUAL DAMASCENE STRUCTURE

SPECIFICATION IDENTIFICATION

The specification of which:

[X] is attached hereto
[ ] was filed on , under Serial No. , executed on even date herewith; or
[ ] Express Mail No.(as Serial No. not yet known)
and was amended on _____ (if applicable)
[ ] was described and claimed in PCT International Application No._____
filed on _____ and as amended under PCT Article 19 on _____.

ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56,

and which is material to the examination of this application; namely, information where there is a substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent, and

[ ] In compliance with this duty there is attached an Information Disclosure Statement in accordance with 37 CFR §1.98.

PRIORITY CLAIM (35 U.S.C. §119)

I hereby claim foreign priority benefits under Title 35, United States Code, §119, of any provisional or foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below, and have also identified below any provisional or foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

[X] No such applications have been filed.

[ ] Such applications have been filed as follows:

A. Prior foreign/PCT application(s) filed within 12 mos. (6 mos. for design) prior to this application, and any priority claims under 35 U.S.C. §119

Country/PCT	Application No	Date Filed	Priority Claimed
			[ ] Yes [ ] No
			[ ] Yes [ ] No
			[ ] Yes [ ] No

B. All foreign application(s), if any, filed more than 12 mos. (6 mos for design) prior to this U.S. application

Country:
Application No:
Filing date:

C. U.S. Provisional Application filed within 12 months prior to this application

Serial No.	Filing Date

PRIORITY CLAIM (35 U.S.C. §120)

I hereby claim the benefit under Title 35, United States Code, §120, of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information that is material to the examination of this application (namely, information where there is substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application.

[X] No such applications have been filed
[ ] Such applications have been filed, as follows:

		Status		
Serial No.	Filing Date	Patented	Pending	Abandoned

POWER OF ATTORNEY

I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

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(713) 623-4844

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and, further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Sec. 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

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Country of Citizenship: FRANCE

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Inventor's signature:_____ Date: 10-24-2000
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Country of Citizenship: P.R. OF CHINA

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Inventor's signature: ______________ Date: 10/23/00

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Country of Citizenship: U.S.A.

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Inventor's signature: ______________ Date: 10/24/00

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Country of Citizenship: U.S.A.

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Inventor's signature: ______________ Date: 24 Oct 00

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U.S.A.

Country of Citizenship: Philippine

(Declaration ends with this page)

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

This declaration is of the following type:

[X] original
[ ] divisional
[ ] continuation
[ ] continuation-in-part

INVENTORSHIP IDENTIFICATION

My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

NOVEL INTEGRATION SCHEME FOR DUAL DAMASCENE STRUCTURE

SPECIFICATION IDENTIFICATION

The specification of which:

[X] is attached hereto
[ ] was filed on , under Serial No. , executed on even date herewith; or
[ ] Express Mail No.(as Serial No. not yet known)
and was amended on _____ (if applicable)
[ ] was described and claimed in PCT International Application No._____
filed on _____ and as amended under PCT Article 19 on _____.

ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56,

and which is material to the examination of this application; namely, information where there is a substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent, and

[ ] In compliance with this duty there is attached an Information Disclosure Statement in accordance with 37 CFR §1.98.

PRIORITY CLAIM (35 U.S.C. §119)

I hereby claim foreign priority benefits under Title 35, United States Code, §119, of any provisional or foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below, and have also identified below any provisional or foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

[X] No such applications have been filed.

[ ] Such applications have been filed as follows:

A. Prior foreign/PCT application(s) filed within 12 mos. (6 mos. for design) prior to this application, and any priority claims under 35 U.S.C. §119

Country/PCT	Application No	Date Filed	Priority Claimed
			[ ] Yes [ ] No
			[ ] Yes [ ] No
			[ ] Yes [ ] No

B. All foreign application(s), if any, filed more than 12 mos. (6 mos for design) prior to this U.S. application

Country:
Application No:
Filing date:

C. U.S. Provisional Application filed within 12 months prior to this application

Serial No.	Filing Date

PRIORITY CLAIM (35 U.S.C. §120)

I hereby claim the benefit under Title 35, United States Code, §120, of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information that is material to the examination of this application (namely, information where there is substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application.

[X] No such applications have been filed
[ ] Such applications have been filed, as follows:

		Status		
Serial No.	Filing Date	Patented	Pending	Abandoned

POWER OF ATTORNEY

I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

Donald Verplancken	Registration No. 33,217
Michael B. Einschlag	Registration No. 29,301
Peter J. Sgarbossa	Registration No. 25,610
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DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and, further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Sec. 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Full name of **sole or first** inventor: FREDERIC GAILLARD

Inventor's signature: _____ Date: 10/31/2000

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Full name of **second** inventor: LI-QUN XIA

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Full name of **third** inventor: ELLIE YIEH

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Full name of **fourth** inventor: PAUL FISHER

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Inventor's signature:____________________ Date:__________
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(Declaration ends with this page)